(2)

TO: ANDY FOX

FROM: S. ESPY

SUBJ: TECHNICAL PROGRESS FOR IDDGA - OBP UPGRADE

The following paragraphs describe progress that has been made since 7/15/90.

TOPIC 1 - OBP-80 PRINTED CIRCUIT BOARD DESIGN

The design of the CPU board is progressing. We had previously selected Microwire technology to implement the board design for several reasons:

1. Controlled Impedence - Since the Multiwire board is drawn wire in epoxy over a copper plane, it is relatively easy to create striplines for everly signal line in the design. The attached technical documentation (Figures 1,2) has been provided by PCK Technology, a company owned by Kollmorgen Corporation.

2. Thermal Transfer Efficiency - The thickness of a Microwire board is approximately .050" thick. This very thin board allows for efficient heat transfer to the heat pipe attached to the backside. The combined thickness of the CPU board and the heatpipe will be approximately .175" thick. Figure 3 shows the mechanical dimensioning of the heat pipe, highlighting the card frame currently used in the OBP.

3. Design Maintenance - A distinct advantage of Microwire technology is the ability to control the design release procedure completely via computer. This allows efficient configuration control, with minimal effort required for re-work. Figure 4 is an assembly drawing created within the Mentor Graphics NETED environment. This 'schematic' was created from the assembly drawing for each integrated circuit.

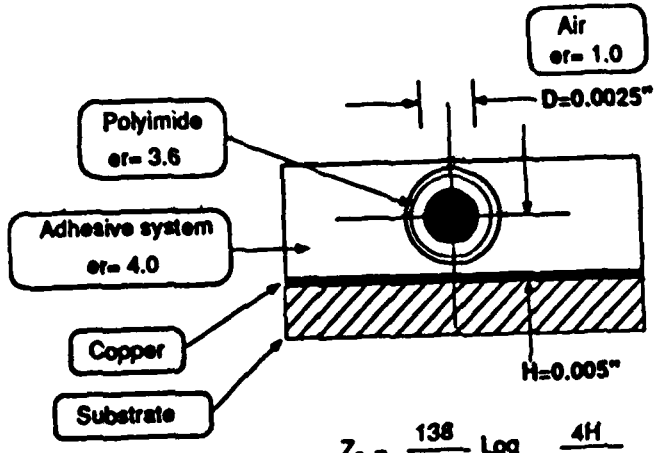
   Martin Marietta used its Internal Research and Development funds to create a netlist extractor for Microwire format. Conventional Mentor schematics which have been annotated to produce a Pin Diagram can be automatically prepared for Microwire input. Figure 5 is a portion of the netlist prepared in this fashion.

TOPIC 2 - S6910 TEST VEHICLE STATUS

The latest test vehicle to be fabricated under Martin Marietta IR&D funds has compleleted fabication at Vitesse. All test structures have successfully passed functional testing. This includes the Programmable Logic Array, the microcode sequencer stack incorporating error correction code, the 16 x 16 2's complement multiplier, and the isolated Latch SEU test cells.

SEU Testing

As discussed at the technical interchange meeting this month, the critical charge for GaAs MESFET structures is well understood. It appears as though the intrinsic data storage elements and the Schottky diode capacitive load exhibit LET's in the 0.92 to 1.5. The latch which



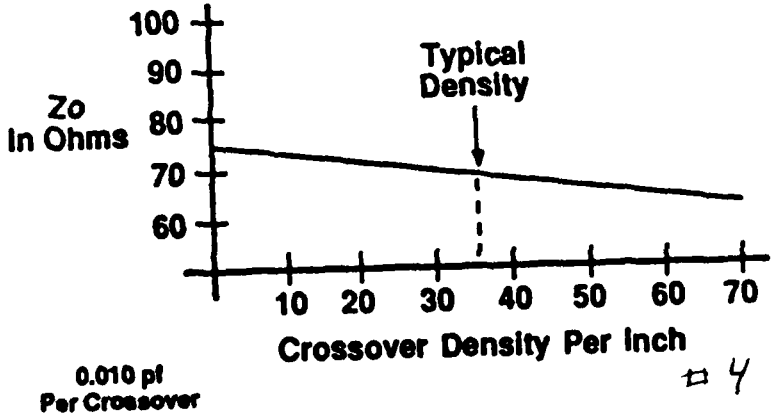
$$Z_o = \frac{138}{\sqrt{er}} \text{Log}_{10} \frac{4H}{D}$$

Where: er= 3.2

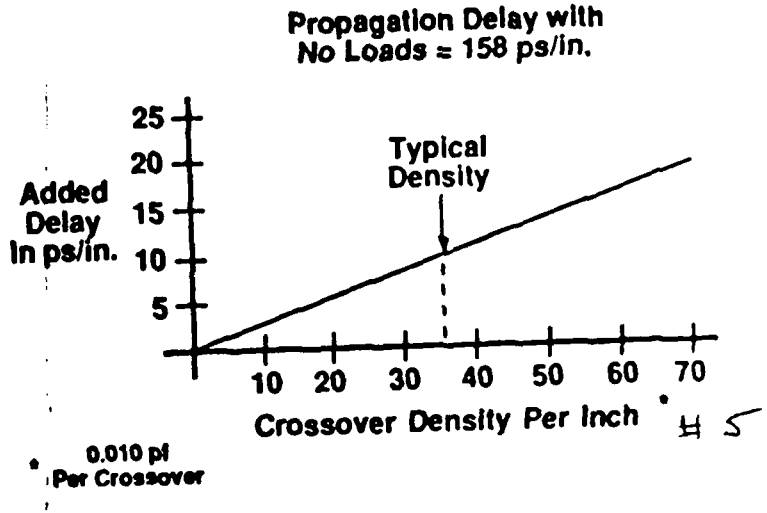
#3

Propagation Delay

Propagation delay for a Microwire signal path is 62 picoseconds/cm which is considerable lower than conventional multilayer circuits built in dual stripline configurations (typically of high density designs). This is due, in part to the epoxy resins used in the Microwire construction that has a low dielectric constant of 4. The other factor leading to this low propagation delay is related to the Microwire construction. Since all interconnection reside on the outside surfaces, the conductors are in a wire over ground configuration, or a sort of microstrip where the conductor is round instead of flat. As a result, the wire is in effect, immersed in a mixed dielectric consisting of epoxy and air where the composite has a dielectric constant of 3.2. Crossover capacitance does have a small effect on the propagation delay, but even in very densely wired circuits the maximum time skew is only 4.7 picoseconds/cm. This can be seen in figure 5.



#4



#5

Figure 1

Crosstalk

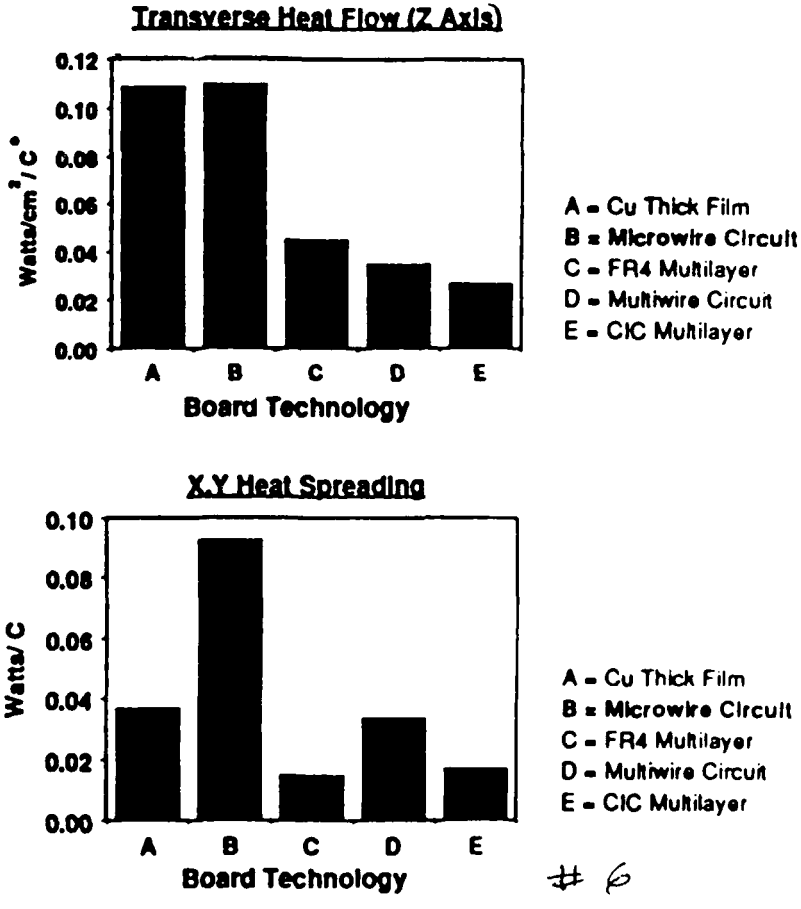
With device rise times decreasing into the sub-nanosecond region crosstalk has become a major consideration in high density circuitry. Traditional approaches for controlling crosstalk have been to space lines far apart or control the parallelism between conductors. Although both of these approaches work, they do not support the goal of producing high density interconnection, since each technique tends to reduce the overall circuit density. The correct approach is to design an interconnection system with relatively low backward crosstalk coefficient that will allow conductor routing with few restrictions while maintaining circuit density. Microwire circuitry meets these requirements with a backward crosstalk coefficient of 5.4% for conductors on 0.31 mm pitch at 75 ohms. This is not surprising when you consider that the conductor is 62 micron in diameter and spaced 5 wire diameters away. This level of crosstalk has been found to be acceptable in most applications. In critical applications limitations can still be placed on parallelism; however, with discrete wiring this task considerably less complex due to an extremely high wire channel capacity and the ease in which wires can be moved in the design process.

One point that can not be overlooked is the advantage of signal routing in all 8 vectors. By routing in both axial and diagonal directions, interconnection density is increased per physical surface without dramatically increasing the potential for more crosstalk, since the diagonal paths are not parallel to the axial wires.

Thermal Performance

One last area to be examined is the thermal performance of Microwire circuits. Two factors contribute to the excellent thermal characteristics of Microwire circuits: The extensive use of metal cores, and the ability to produce an extremely thin interconnection layer. Metal cores play an important role in heat removal however, the key to minimizing the amount of metal used in the core, is to reduce the Z axis thermal resistance of the interconnection layer. Here discrete wiring has a tremendous advantage. Since all the interconnection resides on the outside surfaces of the circuit on a single thin layer, the thermal path to the core is very short thus reducing the thermal resistance in the Z axis.

Z axis thermal resistance can further be reduced through the use of thermal vias. Thermal vias are small holes placed under the devices and plated with copper. Their purpose is to conduct heat form the device to the first copper plane within the circuit. As a result thermal via bypass the epoxy dielectric acting as a thermal shunt.



6

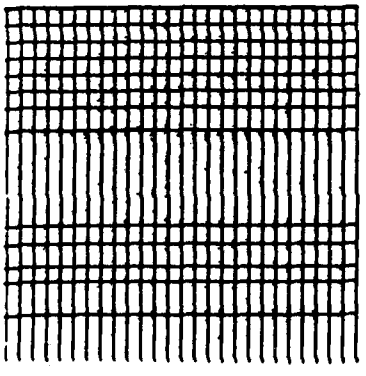
Figure 2

By pa call

Dist	Avail Stock Special
A-1	

VG

STATEMENT "A" Per Andrew Fox
NRL/Code 8120
TELECON
9/24/90



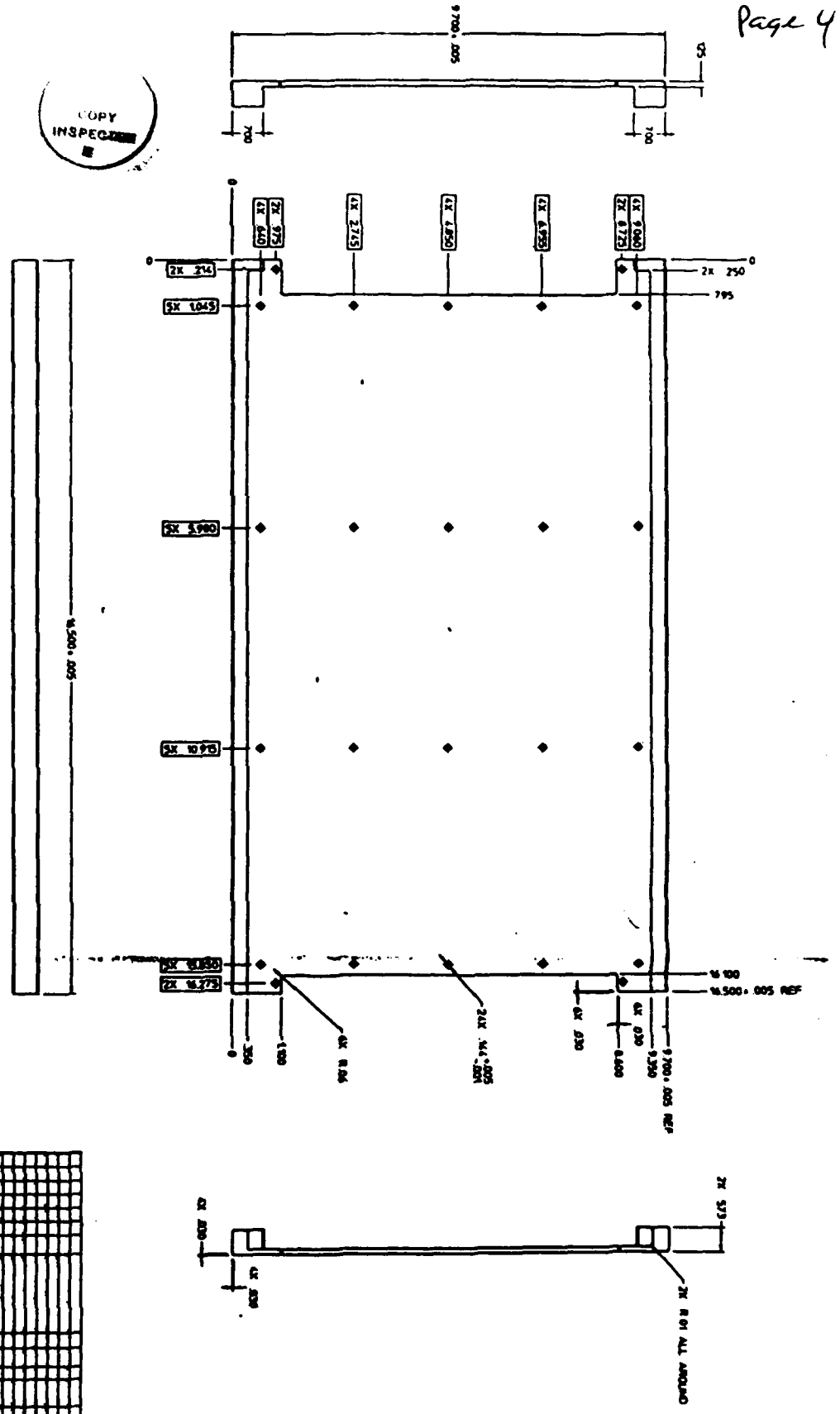


Figure 3

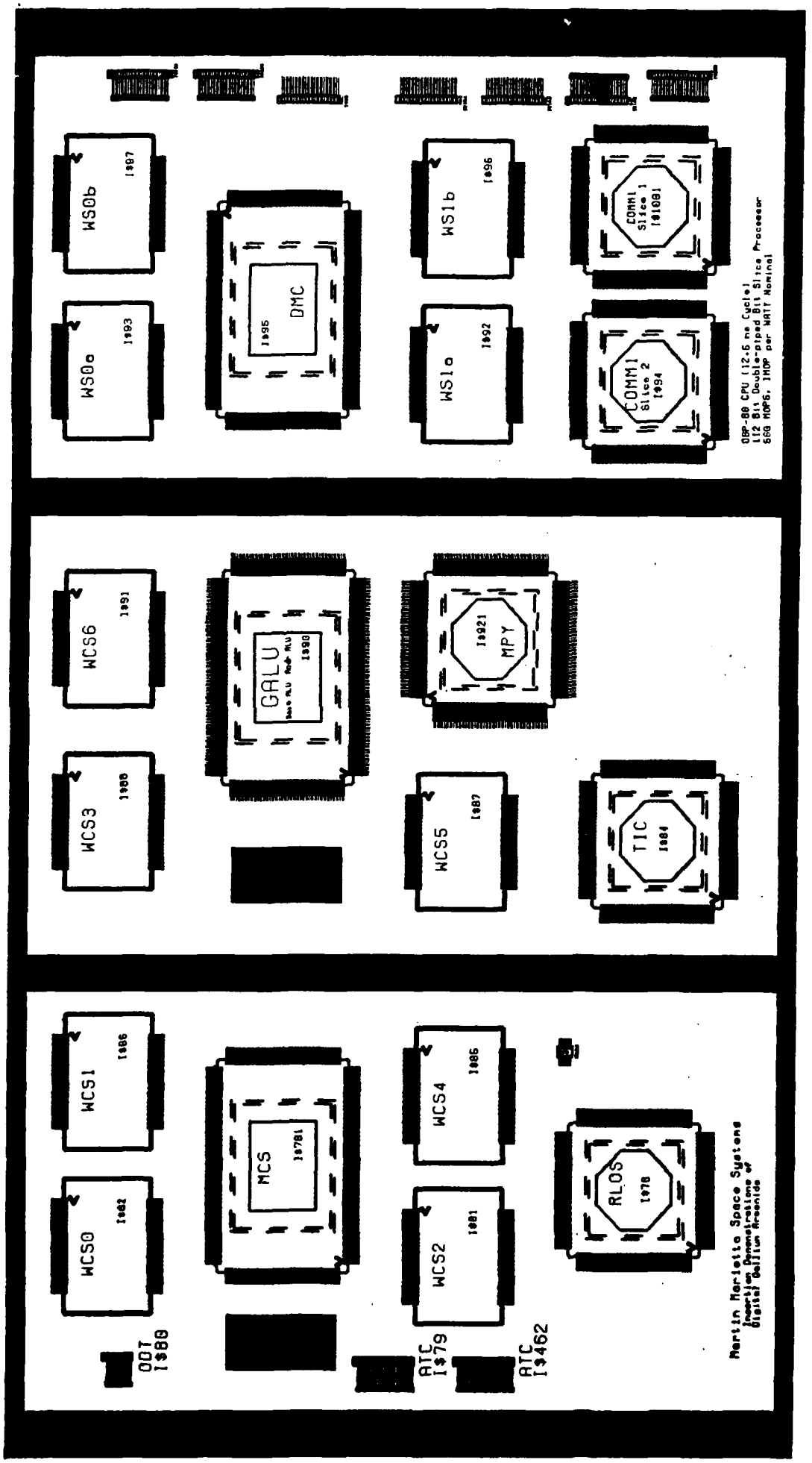

WS0b
WS0a
DMC
WS1b
WS1a
COMM1
Slice 1
COMM1
Slice 2
WCS6
WCS3
GALU
MPY
WCS5
TIC
WCS1
WCS0
MCS
WCS4
WCS2
RLOS
ODT
I$80
ATC
I$79
ATC
I$462
Martin Marietta Space Systems
Insertion Demonstration of
Digital Optics Ensemble

Figure 4

```
ADDR(5)          U#97-9, U#96-9, U#95-217, U#93-9, U#92-9, U#90-101;
ADDR(6)          U#97-8, U#96-8, U#95-216, U#93-8, U#92-8, U#90-100;
ADDR(7)          U#97-7, U#96-7, U#95-215, U#93-7, U#92-7, U#90-99;
ADDR(8)          U#97-6, U#96-6, U#95-214, U#93-6, U#92-6, U#90-97;
ADDR(9)          U#97-5, U#96-5, U#95-213, U#93-5, U#92-5, U#90-96;
ADDR(10)         U#97-4, U#96-4, U#95-212, U#93-4, U#92-4, U#90-95;
ADDR(11)         U#97-3, U#96-3, U#95-211, U#93-3, U#92-3, U#90-94;
ADDR(12)         U#95-210, U#90-92;
ADDR(13)         U#95-209, U#90-89;
ADDR(14)         U#95-208, U#90-88;
ADDR(15)         U#95-207, U#90-87;
DEST(11)         U#95-193, U#921-211, U#90-70, U#781-179;
DEST(12)         U#95-192, U#921-212, U#90-68, U#781-178;
DEST(13)         U#95-191, U#921-213, U#90-67, U#781-177;
DEST(14)         U#95-188, U#921-214, U#90-66, U#781-171;
DEST(15)         U#95-187, U#921-217, U#90-65, U#781-170;
DIN(0)           U#97-44, U#96-44, U#95-28, U#93-44, U#92-44;
DIN(1)           U#97-43, U#96-43, U#95-27, U#93-43, U#92-43;
DIN(2)           U#97-42, U#96-42, U#95-26, U#93-42, U#92-42;
PIPE(64)         U#921-10, U#90-180, U#85-103;
PIPE(65)         U#921-9, U#90-179, U#85-102;
PIPE(66)         U#921-8, U#90-178, U#85-101;
PIPE(67)         U#921-7, U#90-177, U#85-100;
PIPE(68)         U#921-5, U#90-173, U#85-99;
PIPE(69)         U#85-98;
PIPE(70)         U#85-97;
SAVLD            U#781-169;
SB(0)            U#97-67, U#96-67, U#93-67, U#92-67;
SB(1)            U#97-66, U#96-66, U#93-66, U#92-66;
SB(2)            U#97-65, U#96-65, U#93-65, U#92-65;
SB(3)            U#97-61, U#96-61, U#93-61, U#92-61;
SB(4)            U#97-60, U#96-60, U#93-60, U#92-60;
SB(5)            U#97-59, U#96-59, U#93-59, U#92-59;
SB(6)            U#97-58, U#96-58, U#93-58, U#92-58;
SB(7)            U#97-57, U#96-57, U#93-57, U#92-57;
SB0(0)           U#95-123, U#87-51, U#85-51, U#781-314, U#81-51;
SB0(1)           U#95-121, U#87-50, U#85-50, U#781-313, U#81-50;
SB0(2)           U#95-120, U#87-49, U#85-49, U#781-312, U#81-49;
SB0(3)           U#95-117, U#87-48, U#85-48, U#781-310, U#81-48;
```

Figure 5

incorporated 'small' (7K Ohm) resistor decoupling exhibited an upset cross section approximately 3.3 times better than the intrinsic or diode protected latches.

Todd Weatherford estimates that the intrinsic latch error rate (for Boron) is approximately 3.28 x 10^{-4} errors/bit-day.

The Brookhaven upset cross section measurements are supported by pulsed picosecond laser testing. Martin Marietta and NRL personnel utilized the laser to upset the target latches as well. They found that the critical charge of the intrinsic latch was approximately 0.06 picocoulombs. This value is also in very good agreement with VSPICE simulations performed early lat year.

The above testing convinces me that hardening individual storage elements will not be a successful method of achieving our SEU specification. We must depend upon the success of system level solutions to this problem. We anticipate that majority vote and Hamming Code will be successful, given the ability to vary the scrub rate of the Arithmetic (MESFET) components with solar weather conditions.

Multiplier Macrocell Testing

The multiplier macrocell is a key element to use for performance testing the speed-power product of integrated circuit macrocells. This is a highly desirable cell to test, since its critical path involves passing through 87 gate delays. However, a multiplier device is extremely difficult to test. The critical path through the multiplier will actually cause the Most Significant Product bit to toggle several times with only a single change to an input. This occurs because the Full Adders in each column of the multiplier array are producing lateral carries from row to row. These delay elements force the output to switch between a zero and one until the last carry arrives, stabilizing the output.

Consider the plot of delay time versus test vector number for a previous version of the multiplier (no carry lookahead) shown in Figure 6. The patterns are those created by the Automatic Test Pattern Generator for providing >99.75% fault coverage at device screening time. These patterns have been augmented with two vectors which measure the critical path, as predicted by Mentor Graphics Quickpath tool. The resulting 'stabilized' delays illustrate the extreme variability of the propagation delays. This variability depends upon the initial state of the multiplier, and the subsequent propagation paths through the array.

By no means are these 330 patterns intended to be a verification of the critical path. Indeed, it is not possible to 'brute force' the critical path via simulation or measurement as there are more than 2^{34} combinations of primary inputs. When you add the delay dependence on the initial state of the multiplier, this set of combinations becomes even more ludicrous.

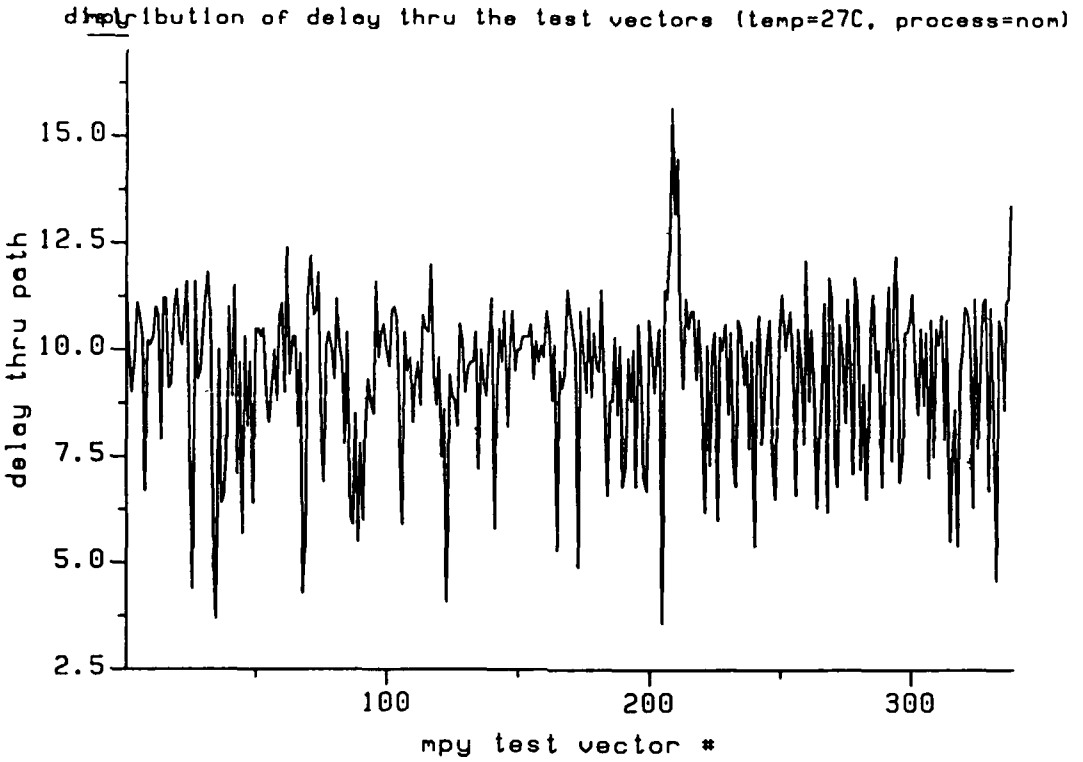


Figure 6 Multiplier Delay vs Sequential Test Vectors

However, the multiplier macrocell can give us crucial information on the timing of the macrocell. The delays of Figure 6 have been re-ordered into the histogram of Figure 7. The small sample size accounts for the distortion in the delay distribution. While we are at Vitesse characterizing this macrocell, we will concentrate on measuring five different delay elements. These are shown in Figure 7 as the black dots.

If the five measurements all track together, then the timing measurements will be used to average the improvement/degradation of each gate. This timing will be used to update the critical path calculation. If all five of the measurements do not track, then the measuement is probably in error due to the inability of the Automated Test Equipment to locate the correct edge transistion. In that event, the measurement will be verified by oscilloscope.

The testing of this macrocell, and the stack timing will be verified in next months status memo, since we have reserved time on the Vitesse ATE early in the month. Initial testing of the macrocells through cut 'n go package test indicates a yield of 14%, which is average for a GaAs die of this size. The die size and density of this chip is about average for the OBP chip set. Therefore, I currently expect to yield 9 good die per 3" wafer .

For production pricing planning concerns, the cost per chip for a wafer run that will yield 45 production devices is approximately $1,178.00 per chip, through screening and burdens. This indicates that an OBP-80 (also in quantity 45) will experience $8,246 in VLSI component costs. Added to this must be the cost associated with flight connectors, PCB's, heat pipes, capacitors, mounting brackets, and heat pipes.

Starting next month, I must begin to develop a cost model for the OBP-80 production units for internal management. It is my intention to price the units based upon an internal production run of 45. To outside sources, we will probably have to enforce a minimum buy of 6 units at a time. This should provide for flight, spare and ground test usage processors. Because of the small internal run, the scrap losses will be high in terms of percentage of production. This will probably mean we will not offer ground units at a reduced price. This follows from the fact we will undoubtedly screen all boards, and the ground units will come from reworked/rejected flight units.

Andy, send any input you may have to me as soon as possible. I'm also assuming that Microwire boards will be flyable. We need to develop a plan which coordinates the testing NRL as done, with the tests we have remaining on the OBP-80 development.

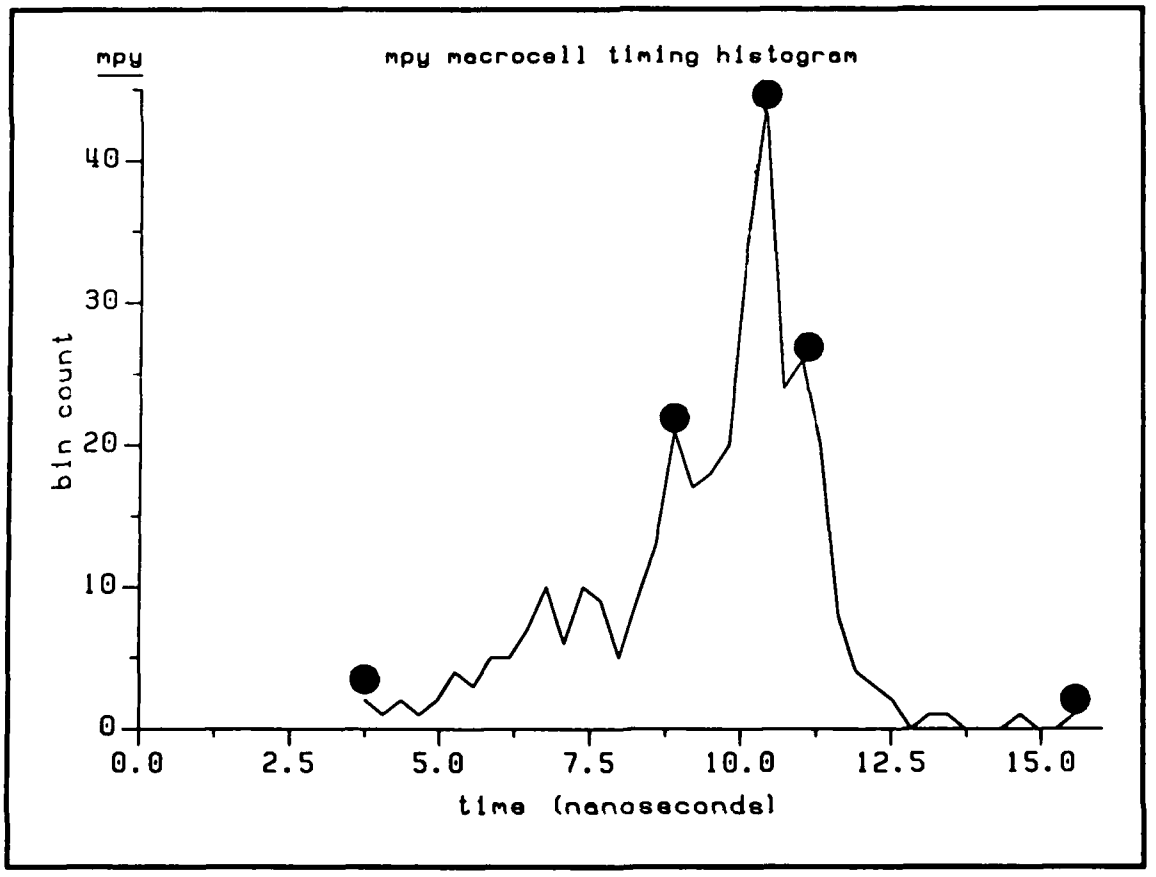


Figure 7 Multiplier Delay Histogram for ATPG Test Vectors

TOPIC 3 - CONTINUED SPD818 TESTING

From the Preliminary Design Review, Martin Marietta received an action item to update the life test projection from 5 years equivalent mission lifetime to 7 years. We had thought that the existing lifetest performed for 4000 hours at 155°C case temperature had accomplished this. The analysis presented at PDR utilized the Arhenius rate reaction equation to predict device ageing. We had utilized the case temperature as a minimum die junction temperature to make the calculation since this avoided the costs of having to measure the junction/case thermal resistance. Equating a lifetest junction teperature of 155°C to mission lifetime at a 125°C junction temperature is about 5 years.

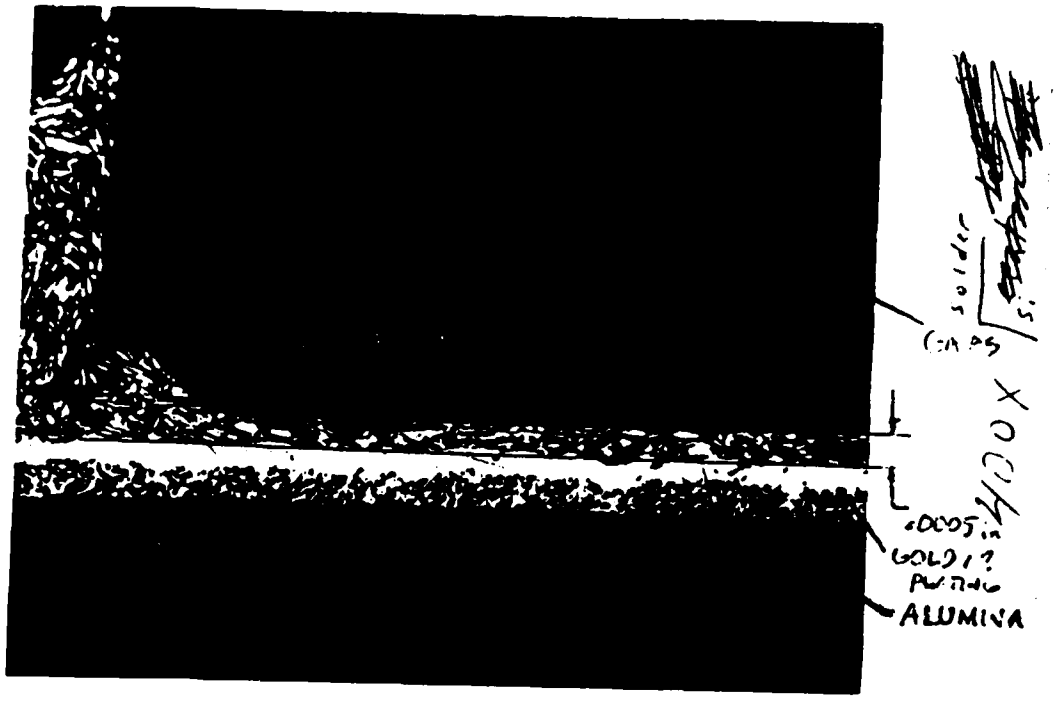
Because the devices consume 1/2 Watt with a die size less than 180 mil/side, we had assumed that the junction temperature would be much higher than that measured at the case. To more closely estimate the juction temperature, three SPD818 devices were delidded. Two devices were selected from the lower power lot, and one from the faster, higher power lot. The three devices were examined with a calibrated Inframetrics Model 600 Imaging Radiometer.

The devices were suspended in air with an ambient temperature of 23.5°C by two 12 guage wires connecting to the VCC and GND pins. The devices were powered up, and the image of Figure 8 was observed. The hottest spot observed came from the die of the center device, which was from the fast lot. A 14.2°C rise over ambient was observed. However, only a maximum temperature difference of 3°C was observed between the die surface and any portion of the ceramic case.

During lifetest, our case temperature was monitored by a thermocouple pinched between the bottom of the case and the zero insertion force socket. This area is directly opposite the die surface, and was a very good indicator of die temperature. The package exhibted a Θ_{JC} of 6 °C/W. Based upon this observation, we cannot equate the existing duration of the lifetest to a 7 year mission at 125°C.

However, the test results did cause us to favorably upgrade our expected mission maximum operating die temperature. The attached photo of a cross sectioned SPD818 package die cavity indicates that the Silver-epoxy die attach process has minimized the thermal transfer distance from the die backside to the case. This was possible because of the small size of the Silver fragments. These fragments allowed the die attach to be compressed to a thickness of approximately 0.0005 in. This is extremely good for epoxy based die attach.

Because of this thermally robust attach process, we estimate that the Θ_{JC} of the 256 pin package will be approximately 0.65 °C/W. This will limit the rise of a 6W part to 4°C. We had previously estimated twice this value. Since we received the cavity up 256 pin packages this month, we will report the actual measurement next month.



If you have any comments or questions regarding this memo, please call me at (303) 971-9276.

Steve Espy

Figure 8